The Effects of "Normal" Annealing Cycles During IGFET Fabrication on Initial and Radiation Induced Gate Insulator Defects

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ABSTRACT

The influence of three typical annealing cycles normally used in IGFET processing on as-fabricated and post-irradiated gate oxide defect levels was studied. These cycles were: 1) "post-oxidation" for 5 minutes at 1000°C in argon, 2) "post-polysilicon" for 30 minutes at 500°C in forming gas, and 3) "post-metallization" for 30 minutes at 400°C in hydrogen. Gate oxide defects were characterized using optically assisted electron injection of n-channel polysilicon-gated IGFET devices. It was found that the presence or absence of any of the three annealing cycles during processing had no effect on measured interface state and bulk oxide defect levels in the as-fabricated devices. Following exposure to Al Kα X-ray radiation, the increase in the number of bulk oxide defects was found to be independent also of the presence or absence of any of the cycles. The interface state density was found to increase only slightly following irradiation, with the smallest increase occurring for devices which had received either the post-oxidation or the post-metal anneal. These results may indicate that other high temperature steps which are present in IGFET processing, as well as the use of different electrode materials than were employed in the earlier studies overshadow the effects of the three annealing cycles studied, and therefore, the entire processing sequence of IGFET fabrication must be considered in determining the factors which influence gate insulator defect levels and susceptibility to ionizing radiation.

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the cycles. The interface state density was found to increase only slightly following irradiation, with the smallest increase occurring for devices which had recieved either the post-oxidation or the post-metal anneal. These results may indicate that other high temperature steps which are present in the IGFET processing, as well as the use of different electrode materials than were employed in the earlier studies overshadow the effects of the three annealing cycles studied, and therefore, the entire processing sequence of IGFET fabrication must be considered in determining the factors which influence gate insulator defect levels and susceptibility to ionizing radiation.

2) As Insulated Gate Field Effect Transistor (IGFET) dimensions continue to decrease, and fabrication sequences rely increasingly on processes which involve ionizing radiation, it becomes essential to understand the radiation-induced threshold voltage shift dependence on gate insulator thickness, since threshold voltage tolerances are required to scale with device dimensions. Unfortunately, the picture that emerges from the literature is unclear in explaining this dependency. In the present study, n-channel IGFET devices were fabricated with gate insulator thicknesses ranging from 6-50 nm, and were then exposed to Al Kα X-ray radiation. Gate oxide coulombic defects and neutral electron traps were measured before and after irradiation using optically assisted electron injection. Following irradiation and injection, the measured voltage shifts indicated that the "extrinsic" defects are localized near, but not at, the Si/SiO_2 interface. It is shown that if the insulator thickness is separated into three regions; (1) a region above the extrinsic defect volume in which ΔV_T is linear in t_{ox}, (2) a region containing all of the extrinsic defects in which ΔV_T is quadratic in t_{ox}, and (3) a region below the extrinsic defect volume close to the Si/SiO_2 interface in which $\Delta V_T=0$, then the ΔV_T vs. t_{ox} data can be very simply explained. This model is shown to be capable of resolving the confusion in the literature surrounding the dependency of ΔV_T on insulator thickness, and of providing a unique and simple method for determining the defect centroid in gate insulators.

1.0 INTRODUCTION

It is well known that the insulators in insulated field effect transistors (MOSFETs or IGFETs) exhibit electrically active defects. The concentration of these defects is reported to be processing dependent[1], and in general the defect concentrations are reported to increase when the insulator is exposed to ionizing radiation.[2,3] In the literature, these defects have been categorized into two groups; interface states and bulk defects.

Interface states, located at the Si/SiO_2 interface by definition, are believed to be the same as the P_B centers found using EPR.[4] These states have the effect of lowering the carrier mobility in the channel of an IGFET, which is realized as a degradation in the transconductance, and sub-threshold slope of the device. Measurements made on metal electroded capacitors have shown that the density of process-induced, "intrinsic" interface states can be reduced by annealing at relatively low temperatures (400°C - 550°C) in a hydrogen containing ambient atmosphere (e.g., H_2 or forming gas), or in an inert ambient atmosphere such as nitrogen or argon when a metal such as aluminum is present over the oxide.[5,6] It is believed that the interfacial traps can become electrically inactive when hydrogen, originating from the ambient atmosphere, or from a reaction of the gate metal with water vapor and/or water in the insulators during the annealing cycle, migrates to the Si/SiO_2 interface and binds the dangling silicon bonds at the P_B centers. In contrast with the effects of low temperature hydrogen annealing on intrinsic interface state densities, it has been reported that the sensitivity of metal electroded capacitors to radiation-induced "extrinsic" interface state formation is increased when high temperature annealing in hydrogen containing ambient atmospheres is included in the fabrication process.[7,8]

Bulk oxide defects have been categorized into four general types; neutral hole traps (NHT), fixed positive charge (FPC), neutral electron traps (NET), and fixed negative charge (FNC).[9] It was reported about 20 years ago that high temperature (600°C - 1200°C) annealing of SiO_2 insulators in inert gas ambient atmospheres will reduce the measured levels of fixed charge in Al-gated MOS capacitors.[10,11] The introduction of charged bulk defects into the insulator, e.g. by exposure to ionizing radiation, will cause a voltage shift of the device, which is usually measured as a flatband voltage shift in capacitors, or a threshold voltage shift in IGFETs. These voltage shifts have been used to measure the radiation sensitivity of insulators which have been subjected to various annealing cycles, and to measure the ability of annealing treatments to remove defects induced by radiation. For

example, it has been reported that the addition of oxygen into the post-oxidation anneal ambient atmosphere reduces the radiation sensitivity of Al-gated MOS capacitors[12], but that annealing of dry oxides in pure N_2 at temperatures above 800°C results in larger voltage shifts in Al-gated capacitors[13], and polysilicon-gated capacitors[14] following irradiation. It has also been reported that low temperature (450°C) annealing of Al-gated capacitors in hydrogen containing ambient atmospheres results in larger post-irradiation flatband voltage shifts.[15] However, low temperature (400°C) annealing in forming gas (10% H_2 - 90% Ar) following exposure to ionizing radiation has been shown to reduce bulk oxide defects in polysilicon-gated IGFETs, with fixed positive charge being more easily annealed than neutral electron traps and fixed negative charge being more difficult to anneal than either.[9]

The present paper is concerned primarily with the role that various annealing cycles which are typically incorporated into the fabrication process of IGFET devices have on the observed defect levels in as-fabricated devices, and in devices subsequently exposed to ionizing radiation, in unbiased polysilicon-gated IGFETs as opposed to biased Al-gated capacitors. Thus, this paper is primarily concerned with IGFET processing-induced defect formation, which includes possible defect formation due to processes which utilize ionizing radiation, e.g. X-ray lithography. It will be shown that some of the annealing cycles which have individually been shown to influence the rad hardness of MOS capacitors essentially have no effect on processing-induced SiO_2 defect formation in IGFETs, perhaps due to the incorporation of other high-temperature processes in the fabrication sequence, or because the initial work was done with biased metal-gated capacitors and modern structures employ polysilicon and/or refractory metal or silicide gate electrodes. Thus, the entire process sequence of an IGFET device must be considered in assessing the factors which govern the initial defect levels and the radiation sensitivity of such devices.

2.0 EXPERIMENTAL PROCEDURE

The devices used in this study were n-channel polysilicon gate IGFETs fabricated on 0.5 ohm-cm (100) p-type silicon wafers. They consist of a large (5×10^{-4} cm^2) enclosed gate insulator area designed specifically for charge injection and radiation damage studies. These devices have been employed in earlier studies.[3,9]. The

process used to fabricate these devices was essentially "radiation-free". Only the reactive ion etching of the polysilicon gate and the ion implantation for the source and drain regions could be considered possible radiation sources.

The gate insulators were so-called "dry-oxides" grown at 1000°C in a O_2 - 4.5% HCl mixture at 1 atmosphere to a thickness of 35 nm. All devices were fabricated simultaneously, with processing splits inserted at various annealing cycle steps in the fabrication sequence. The three annealing cycles involved in the splits were: 1) a "post-oxidation anneal" (POA) for 5 minutes at 1000°C in argon, which is performed as a standard part of the oxidation cycle, 2) a "post-poly anneal" (PPA) for 30 minutes at 500°C in forming gas (8.8% H_2 + 91.2% Ar) which occurs after the dielectric oxide has been deposited over the patterned polysilicon gate electrode but prior to contact hole opening, and 3) a "post-metal anneal" (PMA) for 30 minutes at 400°C in H_2 which is the final processing step. The splits were performed such that one group of wafers received all three of these annealing cycles, another group received none of these cycles, and the other groups received various combinations of them.

Following a complete characterization of the as-fabricated IGFET devices in terms of their initial I-V curves and defect levels, a single quadrant from one wafer in each processing split was exposed to essentially monochromatic Al Kα radiation (1.49 keV) in the X-ray generator described in a previous publication.[16] No gate biasing was used during the irradiation in order to simulate fabrication processes in which ionizing radiation was present. The dose absorbed in the gate insulator was kept constant for all wafers, and was calculated, using the method of reference 17, to be 8.5×10^6 Rads SiO_2. The dosage was calculated using mass absorption coefficients of 1.268×10^3 cm^2/gm and 0.5428×10^3 cm^2/gm, and density values of 2.32 gm/cm^3 and 2.33 gm/cm^3 for SiO_2 and Si respectively.

Device I-V curves were measured prior to irradiation to establish initial threshold voltage values and subthreshold characteristics. It should be noted that all the devices which did not receive the post-metal annealing cycle showed a saturation effect in their I-V curve at intermediate gate voltages, attributable to a high contact resistance in these devices. The post-metal anneal has been found to reduce this contact resistance dramatically following the lift-off metal processing that was used.

Using the method of Benedetto and Boesch[19], subthreshold slope measurements were employed to approximate interface state densities. A measure of the interface state density of an IGFET is the so-called subthreshold "swing", S, defined as:[18,19]

$$S \equiv \ln(10)\,\frac{dV_G}{d\ln(I_D)}, \tag{1}$$

where V_G is the voltage applied to the gate electrode, and I_D is the measured drain current in the subthreshold region of the I-V curve. The quantity $dV_G/d\ln(I_D)$ is the inverse of the slope in the subthreshold region of the I-V curve when the log of the drain current is plotted against the applied gate voltage. The change in the initial and post-irradiation mean interface state density, $\overline{\Delta D_{it}}$, from the weak-inversion to the strong-inversion region of the silicon bandgap is found through the expression:[19]

$$\overline{\Delta D_{it}} = \left[\frac{1}{q}\right]\left[\frac{S'}{S_0} - 1\right]\left[C_i + C_D\right], \tag{2}$$

where S_0 and S' are the initial and post-irradiation subthreshold swings respectively, C_i is the insulator capacitance, and C_D is the maximum depletion-layer capacitance. For the 35 nm oxides in the present study, C_i was calculated to be 9.86×10^{-8} F/cm^2, and using a hole concentration of 2.78×10^{16} cm^{-3} for the 0.5 ohm-cm p-type substrates, C_D was calculated to be 5.48×10^{-8} F/cm^2 at the maximum depletion layer width.

Bulk defect levels were measured before and after irradiation using a modified version of the optically assisted electron injection technique described in reference 20. The number of fixed positive charges (FPC) was determined by measuring the threshold voltage shift following injection of 2.5×10^{13} electrons/cm^2 and the neutral electron trap (NET) concentration was determined by injecting an additional 10^{16} electrons/cm^2 into the same device, and measuring the additional threshold voltage shift. Fixed negative charge (FNC) concentrations, present in small quantities following irradiation, were deduced from a comparison of threshold voltage values before and after irradiation and injection as described previously.[21] If it is assumed that all the defects are located near the Si/SiO_2 interface, and are singly charged, then for the 35 nm oxides a 10 mV threshold voltage shift would correspond to a defect concentration of approximately 0.6×10^{10} cm^{-2}.

3.0 EXPERIMENTAL RESULTS AND DISCUSSION

(1) Interface States

Table I shows the measured initial and post-irradiated subthreshold $dV_G/d\ln(I_D)$ values and the change in the initial and post-irradiation mean interface state density, $\overline{\Delta D_{it}}$, as calculated from Eq. (2) for the various wafer groups. An average value with a $\pm 1\sigma$ variation from the measurement of 5 separate devices in each group is given in the table. The initial $dV_G/d\ln(I_D)$ values are a measure of the interface state density in the as-fabricated devices prior to irradiation. From the initial values in Table I it can be surmised that the initial interface state density, D_{it}^o, is not significant because there is not a significant change in the initial $dV_G/d\ln(I_D)$ values following the post-metal annealing cycle, and this cycle is known to reduce the interface state density when a significant number of interface states are present, as mentioned earlier. The average initial $dV_G/d\ln(I_D)$ prior to post metal annealing (groups 5-8 in Table 1) was 84.4 mV/decade and this average value only slightly decreased to 82.6 mV/decade following post metal annealing (groups 1-4 in Table 1). If these values are substituted into Eq. 2, where now S' is the swing prior to post-metal annealing, and S_0 is the swing after post-metal annealing (which represents the swing value when there are not a significant number of interface states present), then the initial approximate interface state density at mid-gap prior to post-metal annealing is calculated to be $D_{it}^o = 2 \times 10^{10}$ cm^{-2}eV^{-1}. This value is of the order of the sensitivity of the technique, and therefore indicates that within this sensitivity there is not a significant number of interface states present in any of the wafer groups prior to irradiation. Thus, the presence or absence of any or all of the three annealing cycles indicated has little or no effect on the as-fabricated interface state density.

Immediately following irradiation, and prior to a post-irradiation H_2 annealing cycle to remove radiation damage, $dV_G/d\ln(I_D)$ was seen to only slightly increase for most of the groups, with a noticeable increase occurring for the two groups which did not receive either a post-oxidation anneal, or a post-metal anneal. The average calculated $\overline{\Delta D_{it}}$ was approximately 3.4×10^{10} cm^{-2}eV^{-1} at mid-gap for the first six groups which incorporated either, or both the post-oxidation annealing cycle and post-metal annealing cycle, and was 7.4×10^{10} cm^{-2}eV^{-1} for the group which received only the post-poly annealing cycle, and 21.1×10^{10} cm^{-2}eV^{-1} for the group which received none of the three annealing cycles prior to irradiation. Thus, either the post-oxidation

annealing cycle or the post-metal annealing cycle by itself appears to be capable of reducing the subsequent sensitivity to radiation induced interface state formation to its lowest value. The post-poly annealing cycle by itself also reduces this sensitivity, but not to the extent of the other two cycles. Normally, if ionizing radiation was involved during processing (for example at metal level lithography), then post metal annealing would be employed following the exposure to radiation. In the present study we were interested in determining whether or not enhanced susceptibility to radiation could be correlated to the use or non use of annealing cycles of the three types discussed. It is interesting that contrary to the reports[7,8] in which high-temperature H_2 annealing was observed to increase the susceptibility to radiation-induced interface state formation, we find that low-temperature hydrogen annealing somewhat improves radiation sensitivity resistance relative to interface states, with no evidence that any degradation occurs.

(2) Bulk Defects

Table II shows the initial and post-irradiated threshold voltages and threshold voltage shifts following electron injection associated with fixed positive charge, neutral electron traps, and fixed negative charge for the various wafer groups. Initial results shown are averages from 5 separate devices per group, and post-irradiation results are from 10 different devices on the same wafers. All initial FPC voltage shifts were less than 10 mV (the maximum sensitivity of the measurement technique), indicating that the initial fixed positive charge concentration was less than 0.6×10^{10} cm^{-2} independent of whether annealing cycles were used or omitted. The initial large neutral electron trap levels were measured to be about 1.8×10^{10} cm^{-2} for all groups, which is on the low side for this type of defect.

As expected, an increase in these defect levels was observed following irradiation. However, the measured voltage shifts corresponding to these defect levels were essentially the same for all groups, independent of whether the wafers were subjected to any or all of the annealing cycles. The threshold voltage shift values imply that the levels of bulk defects introduced by exposure to 8.5×10^6 Rads were approximately 5.7×10^{11} cm^{-2} for fixed positive charge, 9.4×10^{11} cm^{-2} for neutral electron traps, and 5.4×10^{10} cm^{-2} for fixed negative charge. The approximate 5% variation in the threshold shifts from group to group is typical of the variation seen from one irradiation run to the next.

(3) General Discussion

The above results indicate that the three annealing cycles being studied have little or no effect on the as-fabricated interface state and bulk defect levels, no effect on the sensitivity of the IGFETs to radiation induced bulk defect formation, and only a slight influence on the sensitivity to radiation induced interface state formation. As pointed out, the post metal annealing cycle seems to be useful in reducing contact resistance in lift-off patterned contact barriers, and lift-off metal interconnections, although annealing in hydrogen is not necessary for this beneficial effect to be realized. Yet, as mentioned earlier, these types of annealing cycles by themselves were reported to influence defect levels in MOS capacitors. The difference in the results may be attributable to the differences in processing of the earlier and present devices, as well as to the difference in gate electrode materials employed. Capacitor processing typically only involves oxidation, annealing (optional), metallization and patterning, and possible post-metal annealing. Thus, the addition or subtraction of a particular annealing cycle is a major event which may have noticeable effects on oxide defect levels. On the other hand, IGFET processing is much more involved, typically incorporating 100 or more processing steps. It is therefore possible that other processing steps influence the oxide defect levels to a degree which overshadows the influence of the three annealing cycles studied. In the fabrication sequence used in the present study, the following high-temperature processes following the gate oxidation represent normal parts of our process sequence:

1. Doping of the polysilicon gate to lower sheet resistance
   (900°C for 22 minutes in a $POCl_3$ + Ar ambient atmosphere)

2. "Re-oxidation" of the polysilicon gate and source/drain regions
   (850°C for 30 minutes in a steam H_2O ambient atmosphere)

3. Doping of the dielectric LPCVD oxide layer for step coverage considerations
   (900°C for 22 minutes in a $POCl_3$ + Ar ambient atmosphere)

4. Source/drain drive-in and defect annealing following ion implantation to activate species and remove ion implantation damage
   (1000°C with 5 minutes O_2 + 5 minutes N_2 + 10 minutes Ar)

In essence, all four of the above processing steps also contribute to post-oxidation annealing, even though they

are designed and required for other device considerations. From the results presented, it can be surmised that this combination of processing steps is sufficient in reducing initial oxide defects and radiation sensitivity to the values that were measured. It is also the case, as pointed out, that we used a polysilicon gate technology whereas previous reports were based on metal gate capacitors only. Furthermore, most studies of MOS capacitors, including those referenced earlier, employ biasing during irradiation. It is not known whether irradiation in the "floating" condition that we employed in order to simulate process induced radiation behavior would also affect the lack of significant differences due to the three annealing cycles studied.

It should be pointed out that had ionizing radiation been introduced into the process after the high temperature steps mentioned above, then as mentioned the post metal annealing cycle would exert significant influence on the residual defect levels as shown in reference 9. Examples of such a situation would include X-ray or electron beam lithography of contact and metal levels, and electron beam metallization.

4.0 CONCLUSIONS

The effects of "normal" processing annealing cycles (post-oxidation, post-polysilicon, and post-metallization) on initial and radiation induced gate insulator defect levels in IGFET devices was studied. Although similar cycles have been reported previously to reduce SiO_2 defect levels in MOS capacitors, it was found in the present study that they had little or no effect on the initial interface state and bulk oxide defect densities in the IGFET devices. Also, the annealing cycles had little or no effect on the sensitivity of the devices to radiation induced bulk defect formation. A slight influence on the susceptibility of completely fabricated devices to radiation induced interface state formation was observed, and it was found that either the post-oxidation annealing cycle or the post-metal annealing cycle alone was capable of reducing the susceptibility to its lowest value. The presence of the post-poly annealing cycle by itself in the process also reduced the number of interface states produced subsequently by exposure of the devices to ionizing radiation, but not to the extent of the other two cycles. In lift-off processing the post metal annealing cycle, while not affecting insulator defect levels, was found useful for minimizing contact resistance problems.

The difference in the effect of these annealing cycles on MOS capacitors and IGFET devices is not surprising when the entire processing sequence is considered. Several high temperature processes present in IGFET fabrication, but not in MOS capacitor fabrication (for example, source-drain annealing and impurity activation) contribute to post-oxidation annealing and overshadow the effects of the three annealing cycles studied. In addition, different electrode processes were employed in the earlier work than are used today. Thus the entire processing sequence of IGFET fabrication must be considered in determining the factors which influence gate insulator defect levels and susceptibility to ionizing radiation. In light of the results presented in this paper, it is also obvious that the value of the three annealing cycles studied must be reconsidered since they add additional expense, impact the thermal budget, and can possibly contribute to yield loss in an IGFET fabrication process. Perhaps the most significant conclusion that can be drawn, is that capacitor behavior is probably not representative of what the full transistor behavior is likely to be, and correlations must be treated as suspect unless direct comparison data exists to demonstrate the validity of such correlations.

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TABLES

Table I. Initial and post-irradiated subthreshold inverse slopes and the calculated change in mean interface state density for the various wafer groups. POA = post-oxidation anneal (5 minutes at 1000°C in argon), PPA = post-poly anneal (30 minutes at 500°C in forming gas), and PMA = post-metal anneal (30 minutes at 400°C in hydrogen). The radiation used was Al Kα X-rays to a dose of 8.5 x 10^6 Rads SiO_2.

Group	POA	PPA	PMA	$\frac{dV_G}{d\ln I_D}$ initial (mV/decade)	$\frac{dV_G}{d\ln I_D}$ post irradiation (mV/decade)	$\overline{\Delta D_{it}}$ ($cm^{-2}eV^{-1}$)
1	YES	YES	YES	82.7±0.2	86.1±0.6	3.9×10^{10}
2	YES	NO	YES	82.9±0.3	85.7±0.1	3.2×10^{10}
3	NO	YES	YES	83.0±0.1	85.3±0.1	2.6×10^{10}
4	NO	NO	YES	81.9±0.2	84.8±0.1	3.4×10^{10}
5	YES	YES	NO	84.6±0.7	88.8±0.7	4.7×10^{10}
6	YES	NO	NO	84.3±0.4	86.6±0.2	2.6×10^{10}
7	NO	YES	NO	85.3±0.6	91.9±1.7	7.4×10^{10}
8	NO	NO	NO	83.3±0.8	101.7±2.2	21.1×10^{10}

Table II. Initial and post-irradiated threshold voltages, V_T, and threshold voltage shifts associated with fixed positive charge, ΔV_T(FPC), neutral electron traps, ΔV_T(NET), and fixed negative charge, ΔV_T(FNC), for the various wafer groups. POA = post-oxidation anneal (5 minutes at 1000°C in argon), PPA = post-poly anneal (30 minutes at 500°C in forming gas), and PMA = post-metal anneal (30 minutes at 400°C in hydrogen). The radiation used was Al Kα X-rays to a dose of 8.5 x 10^6 Rads SiO_2.

Group	POA	PPA	PMA	Initial Results			Post-Irradiation Results			
				V_T (volts)	ΔV_T(FPC) (volts)	ΔV_T(NET) (volts)	V_T (volts)	ΔV_T(FPC) (volts)	ΔV_T(NET) (volts)	ΔV_T(FNC) (volts)
1	YES	YES	YES	1.14±.01	.00±.00	.03±.01	0.26±.02	0.97±.03	1.60±.04	0.09±.01
2	YES	NO	YES	1.12±.01	.00±.00	.03±.01	0.27±.01	0.94±.01	1.67±.02	0.09±.01
3	NO	YES	YES	1.12±.01	.00±.00	.03±.00	0.32±.02	0.89±.02	1.52±.03	0.08±.01
4	NO	NO	YES	1.09±.02	.00±.00	.03±.01	0.18±.02	1.01±.02	1.60±.03	0.09±.01
5	YES	YES	NO	1.12±.01	.00±.00	.03±.00	0.25±.10	0.96±.10	1.48±.03	0.08±.01
6	YES	NO	NO	1.11±.01	.00±.00	.03±.00	0.27±.04	0.94±.04	1.46±.03	0.09±.01
7	NO	YES	NO	1.12±.01	.00±.00	.03±.00	0.35±.02	0.88±.02	1.59±.03	0.09±.01
8	NO	NO	NO	1.09±.01	.00±.00	.03±.01	0.22±.02	0.98±.02	1.59±.03	0.10±.01